[Total No. of Questions - 9] [Total No. of Printed Pages - 2]

May-24-0379

CS-303 (Computer Architecture & Organization)

[CSE, IT]

B.Tech. 3rd (CBCS)

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt one question each from section A, B, C & D. Section E is compulsory. Each question carry equal marks.

SECTION - A

1. (a) Explain the basic block diagram of computer. Is it viable to put two counter in Von Neumann model based computer? (5)

   (b) What is a decoder? Compare a decoder and a De-multiplexer. (5)

2. What is instruction format? Discuss different types of instruction formats. (10)

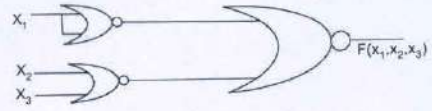
SECTION - B

3. (a) Construct a 4 × 1 multiplexer using logic gates. Obtain 8 × 1 multiplexer with a dual 4 line to 1 line multiplexer having separate enable inputs but Common select lines. (5)

   (b) Explain, with examples, Fixed-point representation. (5)

4. A two level NOR-NOR realization of some expression is shown in fig. Determine the Boolean expression and express it in SOP

form. Construct the truth table of the following circuit and realize using NAND gates. (5+5=10)



SECTION - C

5. (a) Explain direct memory. (5)

   (b) What does DMA stand for? Assume that a processor receives an interrupt request and a DMA request at the same time, which request does the processor process first? Why? (5)

6. (a) Explain Booth's algorithm. Explain with flow chart of it. (5)

   (b) What is race condition? Explain JK flip flop and its truth table. (5)

SECTION - D

7. (a) What is an interrupt? How is it generated? How are interrupts serviced by CPU? (5)

   (b) Explain, in detail, the Reduced Instruction Set Computer Architecture. (5)

8. Discuss various addressing modes in a computer with the help of examples. (10)

SECTION - E (Compulsory)

9. Define following:
   (a) Pipeline depth.
   (b) HIT ratio.
   (c) Hardwired vs Micro-coded control.
   (d) RISC Vs CISC.
   (e) Associative mapping. (5×4=20)