[Total No. of Questions - 9] [Total No. of Printed Pages - 3]

DEC-25-0032

EEEPC-312/ ECEPC-312 (Digital System Design
(EEE, ECE, CSE))

B.Tech.-3rd NEP

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note: Attempt five questions in all, select one question each from section A, B, C, D. Section E (Question-9) is compulsory.

Section-A

1. (a) Implement the following Boolean function **F**, together with the don't-care conditions **d**, using NOR gates only:

$F(A, B, C, D) = \Sigma(2,4,10,12,14)$

$d(A, B, C, D) = \Sigma(0,1,5,8)$ (6)

(b) Simplify the following Boolean function, using 5 variable K-map:

$F(A, B, C, D, E) = \Sigma(1,2,3,5,7,11,13,17,19,23,29,31)$ (6)

2. (a) What are degenerate and non-degenerate forms? List and explain the eight degenerate two-level forms and show that they reduce to a single operation. (6)

(b) What is Hamming code? How are Hamming codes obtained? Observe and rectify the error, if any, in the following 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory?

(i) 000011101010

(ii) 101111110100 (6)

Section-B

3. Describe the analysis of a half-adder and full adder circuit with appropriate truth table, and functions. Implement the following four Boolean expressions with three half adders:

$D = A \oplus B \oplus C$

$E = \bar{A}BC + A\bar{B}C$

$F = AB\bar{C} + (\bar{A} + \bar{B})C$

$G = ABC$ (12)

4. Explain the functionality of decoder. A combinational circuit is specified by the following three Boolean functions:

$F_1(A, B, C) = \Sigma(1, 4, 6)$

$F_2(A, B, C) = \Sigma(3, 5)$

$F_3(A, B, C) = \Sigma(2, 4, 6, 7)$

Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates. (12)

Section-C

5. (a) Illustrate the analysis of SR flip-flop using minimum NAND/NOR gates with appropriate truth table, characteristic equation, excitation table derivations. (6)

(b) Convert a *D flip – flop* into a *JK flip – flop*. (6)

6. Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design. (12)

[P.T.O.]

Section-D

7. Explain how a Finite State Machine (FSM) can be modeled using VHDL. Discuss the key components of an FSM, and provide an example of both a Mealy and a Moore machine. How do state transitions occur in these models? (12)

8. Write and explain the VHDL code for a 4-to-1 multiplexer using both behavioral and structural modeling styles. What are the key differences in the code and how does each approach influence synthesis? (12)

Section-E (Compulsory)

9. Answer following questions in brief: (6×2=12)

   a) Represent the decimal number 2168 in (i) Binary, (ii) BCD. (c) excess-3 code, (d) Gray code.

   b) Add the following BCD numbers:
   (i)10010010 and 01011001 and (ii) 10010111 and 00110111

   c) Explain the functionality of a *Multiplexer.*

   d) Write a short note on *Master-Slave JK Flip-flop.*

   e) What is *TTL NAND* gate?

   f) Differentiate between synchronous and asynchronous counters. State one example of each.