[Total No. of Questions - 9] [Total No. of Printed Pages - 2]

Dec-24-0313 (CBCS)

CS-303 (Computer Architecture & Organization) [CSE, IT]

B.Tech. 3rd

Time : 3 Hours Max. Marks : 60

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt one question from each section. Section E is compulsory. Each question carry equal marks.

SECTION - A

1. (a) Explain the basic block diagram of computer. Is it viable to put two counter in Von Neumann model based computer? (5)

   (b) Construct a 4×1 multiplexer using logic gates. Obtain 8×1 multiplexer with a dual 4 line to 1 line multiplexer having separate enable inputs but Common select lines. (5)

2. (a) What is instruction format? Discuss different types of instruction formats. (5)

   (b) Compare the characteristics of SIMD and MIMD. (5)

SECTION - B

3. (a) How the concept of memory hierarchy make the balance in efficiency and economy of computer? (5)

   (b) Define stack with applications. Show how a stack can be implemented using auto-increment and auto-decrement addressing modes. (5)

4. Consider a machine with a byte addressable main memory of 220 bytes, block size of 16 bytes and a direct mapped cache having 212 cache lines. Let the addresses of two consecutive

bytes in main memory be (E201F)16 and (E2020)16. What are the tag and cache line address (in hex) for main memory address (E201F)16? (10)

SECTION - C

5. (a) Explain fully associative memory mapping. What are the merits and demerits in other cache memory mapping techniques? (5)

   (b) Expiain the communication between DMA and CPU during cycle stealing. (5)

6. (a) Explain Booth's algorithm. Explain with flow chart of it. (5)

   (b) What is race condition? Explain D flip flop and its truth table. (5)

SECTION - D

7. (a) What is an interrupt? How is it generated? How are interrupts serviced by CPU? (5)

   (b) Explain, in detail, the Reduced Instruction Set Computer Architecture. (5)

8. You know that lower the CPI, the better it is, and higher the MIPS, the better it is. Since the CPI of the optimized program increases, and the MIPS decreases, was this really an "optimization"? Explain your answer. (10)

SECTION - E (Compulsory)

9. Define following:

   (a) Cache memory.

   (b) Universal gate.

   (c) Hardwired vs Micro-coded control.

   (d) Machine cycle Vs instruction cycle.

   (e) Hit ratio. (5×4=20)